Reconfigurable optical directed-logic circuits using microresonator-based optical switches

Qianfan Xu[1,*] and Richard Soref[2]

[1]*Department of Electrical and Computer Engineering, Rice University,*
6100 Main Street, MS-366, Houston, Texas 77005, USA
[2]*Sensors Directorate, Air Force Research Laboratory,*
80 Scott Road, Hanscom Air Force Base, Massachusetts 01731-2909, USA
*qianfan@rice.edu

Abstract: We present a reconfigurable optical directed logic architecture that offers several significant improvements over the original directed logic presented by Hardy and Shamir. Specific embodiments of on-chip, waveguided, large-scale-integrated, cellular optical directed logic fabrics are proposed and analyzed. Five important logic functions are presented as examples to show that the same switch fabric can be reconfigured to perform different logic functions.

OCIS codes: (130.3750) Optical logic devices; (250.3140) Integrated optoelectronic circuits; (200.4660) Optical logic.

References and links

1. J. Hardy, and J. Shamir, "Optics inspired logic architecture," Opt. Express **15**(1), 150–165 (2007).
2. L. Zhang, R. Q. Ji, L. X. Jia, L. Yang, P. Zhou, Y. H. Tian, P. Chen, Y. Y. Lu, Z. Y. Jiang, Y. L. Liu, Q. Fang, and M. B. Yu, "Demonstration of directed XOR/XNOR logic gates using two cascaded microring resonators," Opt. Lett. **35**(10), 1620–1622 (2010).
3. Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," Nature **435**(7040), 325–327 (2005).
4. Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," Opt. Express **15**(2), 430–436 (2007).
5. P. Dong, R. Shafiiha, S. Liao, H. Liang, N.-N. Feng, D. Feng, G. Li, X. Zheng, A. V. Krishnamoorthy, and M. Asghari, "Wavelength-tunable silicon microring modulator," Opt. Express **18**(11), 10941–10946 (2010).
6. W. A. Zortman, M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Low-power high-speed silicon microdisk modulators," in *Conference on Lasers and Electro-Optics (CLEO) and Quantum Electronics and Laser Science Conference (QELS),* Technical Digest (CD) (Optical Society of America, 2010), paper CThJ2014.
7. B. Analui, D. Guckenberger, D. Kucharski, and A. Narasimha, "A fully integrated 20-Gb/s optoelectronic transceiver implemented in a standard 0.13-μm CMOS SOI technology," IEEE J. Solid-State Circuits **41**(12), 2945–2955 (2006).
8. O. Schwelb, "Transmission, group delay, and dispersion in single-ring optical resonators and add/drop filters-a tutorial overview," J. Lightwave Technol. **22**(5), 1380–1394 (2004).
9. Q. Xu, J. Shakya, and M. Lipson, "Direct measurement of tunable optical delays on chip analogue to electromagnetically induced transparency," Opt. Express **14**(14), 6463–6468 (2006).
10. R. C. Williamson, "Sensitivity-bandwidth product for electro-optic modulators," Opt. Lett. **26**(17), 1362–1363 (2001).
11. M. A. Popovic, "Resonant optical modulators beyond conventional energy-efficiency and modulation frequency limitations," in *Integrated photonics research, silicon and nanophotonics* (Optical Society of America, 2010), IMC2.
12. J. Liu, J. Michel, W. Giziewicz, D. Pan, K. Wada, D. D. Cannon, S. Jongthammanurak, D. T. Danielson, L. C. Kimerling, J. Chen, F. O. Ilday, F. X. Kartner, and J. Yasaitis, "High-performance, tensile-strained Ge p-i-n photodetectors on a Si platform," Appl. Phys. Lett. **87**(10), 103501 (2005).
13. L. Chen, and M. Lipson, "Ultra-low capacitance and high speed germanium photodetectors on silicon," Opt. Express **17**(10), 7901–7906 (2009).
14. L. Vivien, J. Osmond, J.-M. Fédéli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide," Opt. Express **17**(8), 6252–6257 (2009).
15. S. Assefa, F. Xia, and Y. A. Vlasov, "Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects," Nature **464**(7285), 80–84 (2010).

16. Q. Xu, D. Fattal, and R. G. Beausoleil, "Silicon microring resonators with 1.5-microm radius," Opt. Express **16**(6), 4309–4315 (2008).
17. A. Narasimha, B. Analui, Y. Liang, T. J. Sleboda, S. Abdalla, E. Balmater, S. Gloeckner, D. Guckenberger, M. Harrison, R. G. M. P. Koumans, D. Kucharski, A. Mekis, S. Mirsaidi, D. Song, and T. Pinguet, "A fully integrated 4x 10-Gb/s DWDM optoelectronic transceiver implemented in a standard 0.13 mu m CMOS SOI technology," IEEE J. Solid-State Circuits **42**(12), 2736–2744 (2007).
18. R. A. Soref, and B. R. Bennett, "Electrooptical effects in silicon," IEEE J. Quantum Electron. **23**(1), 123–129 (1987).
19. A. H. Atabaki, E. Shah Hosseini, A. A. Eftekhar, S. Yegnanarayanan, and A. Adibi, "Optimization of metallic microheaters for high-speed reconfigurable silicon photonics," Opt. Express **18**(17), 18312–18323 (2010).
20. M. C. M. Lee, and M. C. Wu, "Tunable coupling regimes of silicon microdisk resonators using MEMS actuators," Opt. Express **14**(11), 4703–4712 (2006).
21. G. S. Wiederhecker, L. Chen, A. Gondarenko, and M. Lipson, "Controlling photonic structures using optical forces," Nature **462**(7273), 633–636 (2009).
22. L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "40 Gbit/s silicon optical modulator for highspeed applications," Electron. Lett. **43**(22), 1196–1197 (2007).
23. Y.-H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller, and J. S. Harris, "Strong quantum-confined Stark effect in germanium quantum-well structures on silicon," Nature **437**(7063), 1334–1336 (2005).
24. C. Kochar, A. Kodi, and A. Louri, "Proposed low-power high-speed microring resonator-based switching technique for dynamically reconfigurable optical interconnects," IEEE Photon. Technol. Lett. **19**(17), 1304–1306 (2007).
25. Q. Xu, V. R. Almeida, and M. Lipson, "Micrometer-scale all-optical wavelength converter on silicon," Opt. Lett. **30**(20), 2733–2735 (2005).
26. A. G. J. S. Levy, M. A. Foster, A. C. Turner-Foster, A. L. Gaeta, and M. Lipson, "Monolithically integrated multiple wavelength oscillator on silicon," arXiv:0907.1077v2 [physics.optics] (2009).
27. J. Van Campenhout, L. Liu, P. Rojo Romeo, D. Van Thourhout, C. Seassal, P. Regreny, L. D. Cioccio, J.-M. Fedeli, and R. Baets, "A compact SOI-integrated multiwavelength laser source based on cascaded InP microdisks," IEEE Photon. Technol. Lett. **20**(16), 1345–1347 (2008).
28. A. Kovsh, I. Krestnikov, D. Livshits, S. Mikhrin, J. Weimert, and A. Zhukov, "Quantum dot laser with 75 nm broad spectrum of emission," Opt. Lett. **32**(7), 793–795 (2007).
29. A. Gubenko, I. Krestnikov, D. Livshtis, S. Mikhrin, A. Kovsh, L. West, C. Bornholdt, N. Grote, and A. Zhukov, "Error-free 10 Gbit/s transmission using individual Fabry-Perot modes of low-noise quantum-dot laser," Electron. Lett. **43**(25), 1430–1431 (2007).

1. Introduction

The purpose of this paper is to present a new optical directed logic (DL) architecture that is based on a regular array of optical switches. The same circuit can be reconfigured to perform different logic functions. This new architecture offers significant improvements in reconfigurability and scalability over the original DL proposed by Hardy and Shamir in their pioneering 2007 paper [1].

Speaking generally, DL is an innovative paradigm that minimizes the latency in calculating a complicated logic function by taking advantage of fast and low-loss propagation of light in a highly integrated, waveguided, on-chip photonic system. DL is best applied to real-time applications such as video analysis, recognition-and-analysis of fast-moving objects, and visualization. DL can also provide ultrafast network routing functions that enable highly efficient packet-switched interconnections for high-performance computing. The main task for packet routing is to look up the network address in the routing table. The new architecture we present here can directly and dynamically map a lookup table onto an optical switch fabric and obtain the result with very low delay. In an interconnection network, the lookup table is probably small enough so that the routing function can be realized with the moderate-scale photonic integration capability that has been demonstrated today. Optical DL has the potential to achieve lower latency than state-of-the-art electronic transistor logic.

A DL circuit is formed by an on-chip network of optical switches [2]. The state of each switch is controlled by an input logic signal. While it takes a finite amount of time for each switch to respond to a change in its control signal, all of the switches operate simultaneously and their switching delays do not accumulate—in contrast to electronic transistor logic circuits wherein gate delays are cascaded, resulting in large latency.

We develop in this paper a new DL architecture that is well suited for CMOS-compatible silicon photonics, especially for logic based upon resonant, electro-optical 1×1 and 2×2 optical switches that employ micro-rings or micro-disks whose resonance mode is shifted by the depletion or injection of carriers [3–6]. The idea is to create large-scale integrated (LSI) optical logic "fabrics" (gate arrays) using the small size, fast switching speed and ultra-low power consumption of the micro resonators. In other words, resonant switches are essential enablers of LSI.

Compared to the original DL, the improvements and advantages of our new DL are: (1) a complete cellular geometry for large-scale logic fabrics, (2) much shorter optical paths and therefore better scalability because of parallel path sum-of-products processing, (3) simple row-column layout of a large fabric without any waveguide crossovers, (4) matrix addressing, (5) greater ease of programming, (6) multi-spectral fabrics, and (7) low-cost manufacture of LSI optical DL in a high-volume CMOS-photonics foundry [7]. The new DL is believed to hold the key to reconfigurable optical logic systems such as the optical "field programmable" gate arrays. In this paper, five important logic functions are used as examples to show that the same switch fabric can be reconfigured to perform different logic functions.

2. Background

Optical computing has a long and diverse history. In our opinion, the future of optical computing resides in four areas: digital optical logic (the topic of this paper), quantum computing, analog-and-digital optical signal processing, and photonic reservoir computing that involves nonlinear elements, neural networks and training sets.

The original DL paradigm proposed in [1] is an innovative way of performing digital optical logic. In that design, at least three 2×2 optical switches are required to perform a two-input logic operation. To calculate a complex function, the number of switches needed scales super-linearly with the total number of logic operations in the function. These switches are cascaded in such a way that light has to propagate through a long chain of switches in the worst case scenario, which poses a significant limitation on the scalability of the original DL paradigm.

The long optical path can be a problem both in terms of the latency and the insertion loss. The longer physical length of the circuit will be translated into a longer delay. In addition, when optical micro-resonators are used as the 2×2 switches, light going to the cross port of the switch experiences an additional delay determined by the photon lifetime of the resonator, which is on the order of picoseconds. Thus cascading a large number of 2×2 switches can result in a large latency that is comparable to electronic transistor logic. Note that the delay we discuss here is the group delay experienced by the lightwave when the switch is in steady state [8,9], which is due to the phase response associated with the resonance peak. This is different from the switching time limit imposed by the photon lifetime [10], which is of a lesser concern here because that the switching time does not accumulate, and that this limit can be overcome with a special switching mechanism [11]. The number of switches in an optical path is also limited by the insertion loss of the 2×2 switches, which is usually non-negligible for the cross port.

Here we propose a two-stage structure wherein a large number of parallel optical paths are used, thereby significantly reducing the length of each path. Besides that, only 1×1 switches (on/off switches) are necessary to form the switch fabrics. A 1×1 switch can be built based on the through port of a micro-resonator, which has both low delay [8] and low loss. That is because when light can pass the switch, it does not interact with the resonator; and when light is coupled into the resonator, the optical power is dropped. In either case, the output of the switch is not affected by the optical delay and optical loss in the resonator. The lower latency and loss in each optical path significantly improves the scalability of the proposed architecture when compared to the original DL paradigm. While the optic-to-electric (O/E) conversion between the two stages introduces an additional latency, this latency is small with the compact

and integrated photodetectors, and this latency does not scale with the size of the logic. We will also show alternative implementations where the O/E conversion module is not needed.

The goals of this paper are: (1) to develop the reconfigurable and cellular realization of DL with high scalability, (2) to present practical photonic realizations of the unit cells based on ultra-small semiconductor waveguided optical switches, and (3) to give specific examples of important combinational logic fabrics to demonstrate the value of our proposed reconfigurable cellular fabric.

Our approach–the themes of this paper–are reconfigurability, waveguided components and interconnections, scalability, very low latency, on-chip planar integration, wavelength-multiplexed fabrics, and large scale integration. The minimized latency implies that the optical loss for light propagating across the entire logic fabric will be relatively low, obviating the need for semiconductor optical amplifiers.

We would like to suggest that the approach just cited can be exploited in all four optical computing areas listed above (not just in logic) leading to many advances there.

3. Logic architecture

Any combinational logic function can be written in a sum-of-products format. Each product is an AND function of the input logic signals, where each input signal appears only once in either its inverted or noninverted form. The sum is the result of an OR function of all the products. The sum-of-products expression of a logic function can be mapped onto a two-stage directed-logic circuit shown in the block-diagram of Fig. 1 where the first stage calculates all the products, and the second stage calculates the sum of the products.
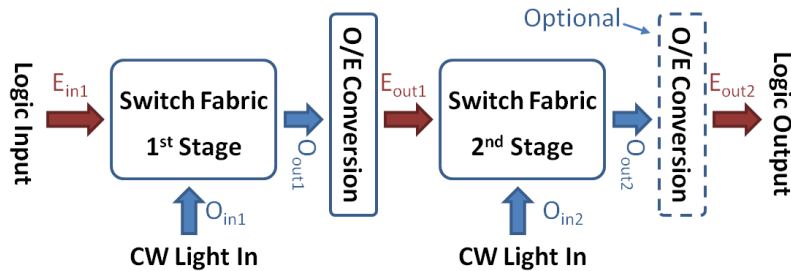

Fig. 1. Block diagram of the reconfigurable directed logic circuit.

Each stage is formed by an array of parallel optical waveguides. Each waveguide passes through an array of identical and reconfigurable 1×1 optical switches controlled by the logic input signals. Each optical switch is in either the *pass* or the *block* state depending on the logic signal applied to it and the operation mode in which this switch is configured. In between the two stages, an optic-to-electric (O/E) conversion module converts the optical output of a waveguide in the first stage to an electrical logic signal that is used to control the optical switches in the second stage. The optical outputs of the second stage give the calculated results of the target logic functions. If desired, they can be converted back to electric logic signals by an optional O/E conversion module.

A continuous-wave (CW) laser is sent into each optical waveguide. Light can pass through the waveguide and thus give an output signal as TRUE ('1') only when all the switches are in the *pass* state. The optical output of this waveguide thus represents a product of the logic inputs. Each 1×1 switch can be reconfigured to be in the *pass* state either when the control signal is TRUE ('1') (the pass/block mode) or when the control signal is FALSE ('0') (the block/pass mode). Correspondingly, the product that the waveguide calculates will include either the noninverted or the inverted control signal. The 1×1 switch can also be reconfigured to a third mode where it is always in the *pass* state no matter what the logic input is (the

pass/pass mode). In this mode, the logic input will not appear in the product that is calculated by this waveguide.

While the OR function is hard to implement directly, we can take advantage of this relationship between OR and NAND functions:

$$A + B = \overline{\overline{A} \cdot \overline{B}} \qquad (1)$$

Equation (1) shows that the inversion of the sum is a product that can be calculated in the same way as discussed above. To take advantage of this, we express the inversion of the target function in the sum-of-products form. Then the target function can be obtained by calculating the product of the inverted products. In the next two subsections, we will use three examples to illustrate this process.

3.1 Eight-bit priority encoder

Here we use an 8-bit priority encoder as the first example to illustrate how a logic function is mapped onto the proposed directed-logic circuit. Figure 2(a) shows the truth table of the encoder whose output, a three-bit binary number, is the index of the first (with the highest index) nonzero logic input.

The directed-logic circuit constructed to perform this function, as shown in Fig. 2(b), is a direct mapping of the truth table. In Fig. 2(b), the black lines represent optical waveguides, while the red lines represent the electrical lines carrying the logic signals. At each cross point of a red line and a black line, there is a reconfigurable 1×1 optical switch that either passes or blocks the optical signal. The optical switch can be configured to be in one of three operation modes. The switches in the pass/block mode that pass the light when logic input is '1' are represented by solid squares. The switches in the block/pass mode are represented by hollow squares. The switches in the pass/pass mode are represented by the dashed circles.

By comparing Fig. 2(a) and Fig. 2(b), one can see that the mapping from the truth table to the directed logic circuit can be done in these two simple steps:

1. The first stage of the logic circuit is mapped from the left side of the truth table. The '1's in the truth table are mapped to switches in the pass/block mode; the '0's are mapped to switches in the block/pass mode; while the 'x's are mapped to switches in the pass/pass mode.

2. The second stage of the logic circuit is mapped from the right side of the truth table. The '1's are mapped to switches in the pass/pass mode while '0's are mapped to switches in the block/pass mode.

To understand this mapping from the sum-of-products expression, we can use the output y_0 as an example. As mentioned before, we should express the inverted output function $\overline{y_0}$ in the sum-of-products form which is

$$\overline{y_0} = \overline{x_7}\,\overline{x_6} + \overline{x_7}\,x_6\,\overline{x_5}\,x_4 + \overline{x_7}\,x_6\,\overline{x_5}\,x_4\,\overline{x_3}\,x_2 + \overline{x_7}\,x_6\,\overline{x_5}\,x_4\,\overline{x_3}\,x_2\,\overline{x_1}\,x_0 \qquad (2)$$

Then, the output y_0 can be written as a product of the inverted products:

$$y_0 = \overline{\overline{x_7}\,\overline{x_6}} \cdot \overline{\overline{x_7}\,x_6\,\overline{x_5}\,x_4} \cdot \overline{\overline{x_7}\,x_6\,\overline{x_5}\,x_4\,\overline{x_3}\,x_2} \cdot \overline{\overline{x_7}\,x_6\,\overline{x_5}\,x_4\,\overline{x_3}\,x_2\,\overline{x_1}\,x_0} \qquad (3)$$

This is the expression that is mapped onto the two-stage directed logic circuit shown in Fig. 2(b).
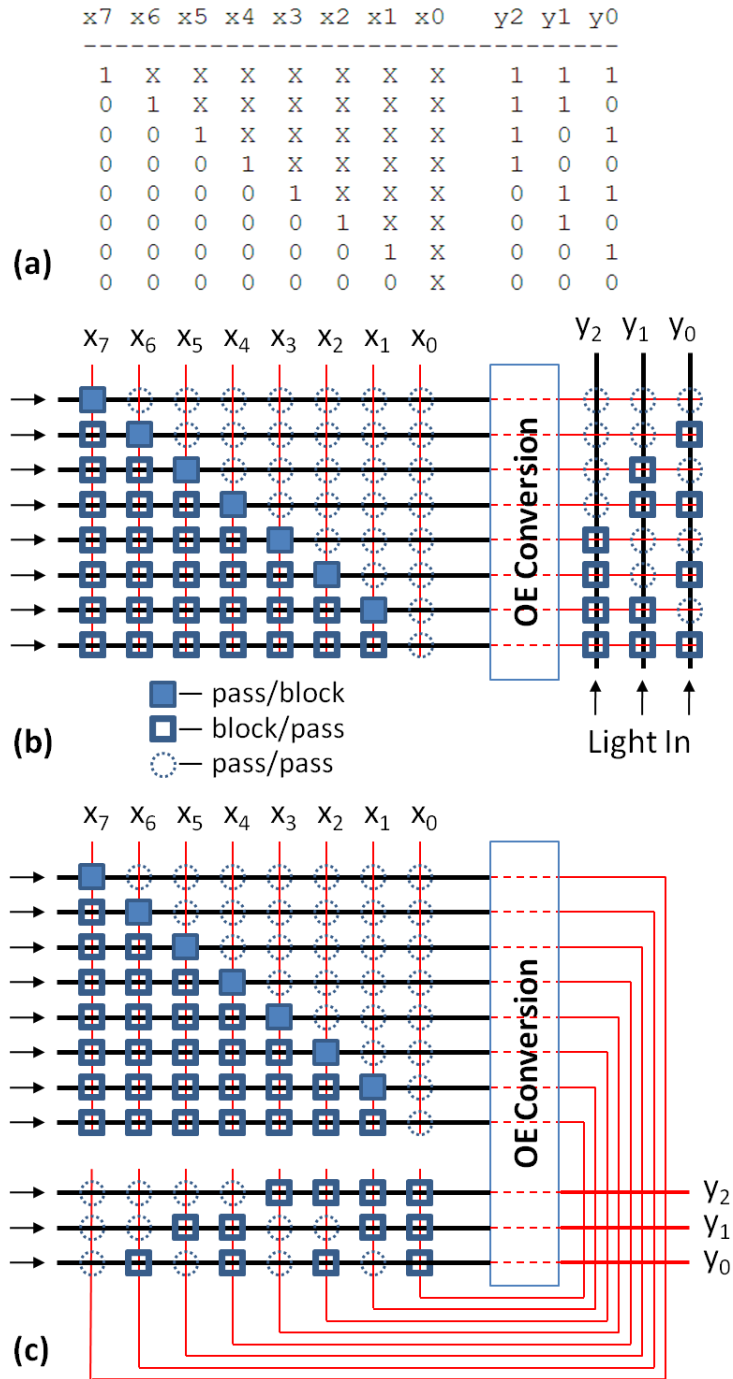
(a)

(b)

(c)

Fig. 2. The truth table and the circuit diagrams of an 8-bit priority encoder. (a) The truth table. 'x' means "any". (b) The directed logic implementation of the encoder. Black lines: optical waveguides; Red lines: electric logic signal controlling the optical switches; Solid squares: optical switches in the pass/block mode, i.e. it passes light when the control logic signal is '1' and blocks light when the control logic signal is '0'; Hollow squares: optical switches in the block/pass mode; Dashed circles, optical switches in the pass/pass mode. (c) An alternative drawing of the same circuit as shown in (b).

While the logic circuit is split into two stages, both of them have the same structure and can be constructed on the same switch fabric. In Fig. 2(c), we show the circuit of Fig. 2(b) drawn in a different way, illustrating that the 2nd stage can be part of the same switch fabric that is used for the 1st stages. In the rest part of the paper, we will continue to draw the circuit in a way similar to Fig. 2(b), since that is clearer logically. However, in all cases, the two stages can be mapped on one switch fabric connected to one O/E conversion module.

3.2 Multiplexing and demultiplexing functions

To show the versatility of this logic architecture, we now use two new examples to demonstrate that the same uniform switch fabric can be reconfigured to perform different logic functions. Figure 3 shows the circuit diagrams of the directed logic circuits that perform 8-to-1 multiplexer (MUX) (a) and 1-to-8 demultiplexer (DEMUX) (b) functions. The MUX selects one of the eight input logic signals according to the binary number $S = s_2s_1s_0$ and sends it to the output ($y = x_S$). The DEMUX, on the other hand, sends the input logic signal to one of its eight outputs according to the binary number $S = s_2s_1s_0$ ($y_S = x$).

One can see that these functions can be realized with switching fabrics of the same structure as that used in the previous subsection. To convert from a particular logic function to another, one needs only to redefine the input and output signals and to reconfigure the operation mode of the 1×1 switches.
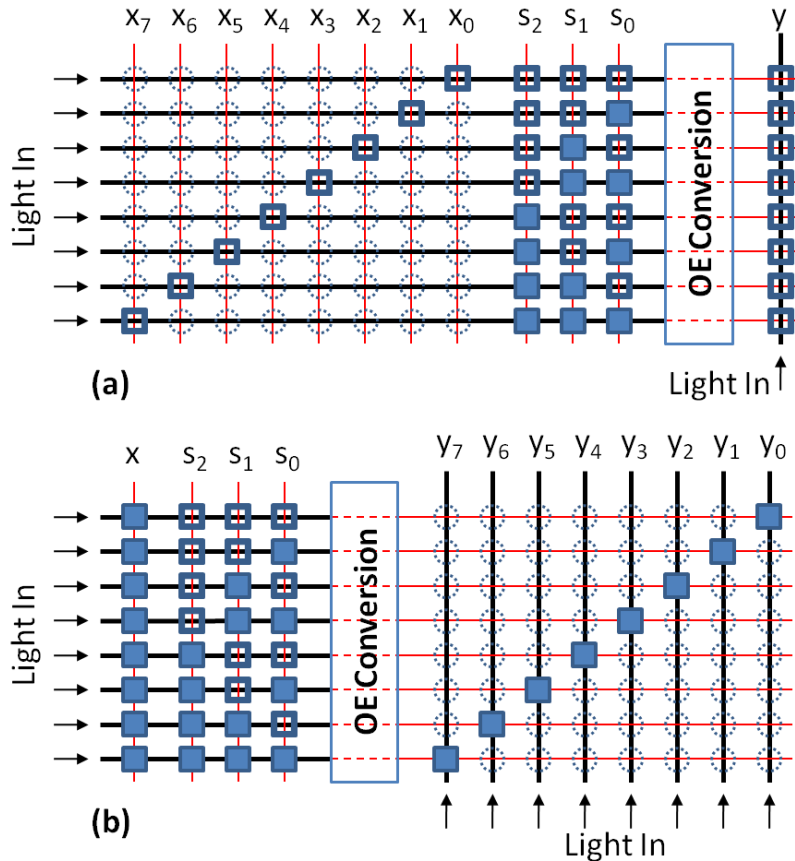

Fig. 3. Circuit diagrams of the directed logic circuits performing 8-to-1 MUX (a) and 1-to-8 DEMUX (b) functions. The meanings of the symbols in the diagram are the same as those in Fig. 2.

3.3 O/E conversion module

The O/E module is a 1D in-line array of efficient photodetectors and associated electronic amplifiers that are easy to manufacture and integrate monolithically with the logic array. For example, in the case of silicon photonics, the O/E converter will be based on a group of identical waveguide-integrated Germanium photodiodes that have high efficiency, high speed and are CMOS compatible [12–15].

4. Switching fabric and the unit cell

The cellular switching fabric employed in the above logic architecture is composed of identical unit cells, and the reconfigurable 1 x 1 switch that constitutes the unit cell can be built based on silicon microring or microdisk resonators. In this subsection, we will show the structure of this switch and show how to implement the three operation modes of the switch.

The ideal optical switches for DL circuits should have small size, fast switching speed, low power consumption and the capability of large-scale integration. The latency of the logic circuit is determined by the overall path length of light and the switching time of a single switch. A compact size for each switch is necessary to reduce the overall path length of the circuit. Since a complex logic circuit may use thousands of switches, a highly integrated solution is required wherein each switch needs to have a very low power consumption.

Optical switches based on silicon micro-resonators are the best fit for directed-logic circuits since they meet all of the criteria listed above. The high refractive-index contrast of a silicon-on-insulator (SOI) platform makes it possible to build very compact micro-resonators, down to sub-wavelength dimensions [16], with high quality factor Q. Optical switches with low switching energy (~3 fJ/bit [6]) can be realized with micro-resonators that have both small mode volume and high Q. Silicon photonics is a leading contender for the most economical platform for large-scale optoelectronic integration. It takes full advantage of the mature silicon process infrastructure. Integrated silicon photonic systems have been fabricated in *commercial CMOS foundries* [17], leading to high yield and low cost.

Figure 4(a) shows an SEM picture of a typical microring resonator having a radius as small as 1.5 μm side-coupled to a straight waveguide [16]. This device is the basis of a 1×1 switch that can be used as the unit cell of the proposed logic architecture. When the light traveling in the straight waveguide resonates with the microring resonator, light couples from the waveguide to the ring, and the optical transmission in the waveguide reach a minimum. Thus, as shown in Fig. 4(c)–4(e), a typical transmission spectrum of a microring resonator shows a sharp dip around the resonant wavelength. By tuning the resonant wavelength of the resonator, the transmission of light at a given wavelength λ_L can be changed from high to low, or vice versa, resulting in the *pass* and *block* states we need for a 1×1 switch.

The resonant wavelength of a microring resonator can be tuned by changing the effective index of the silicon ring. This can be done in numerous ways, including changing the free-carrier density in silicon [18], varying the temperature of the silicon ring with integrated micro-heaters [5,19], or modifying the structural parameters through micromechanical tuning [20,21]. Figure 4(b) shows one example where a p-i-n junction is built across the ring to inject and extract free carriers in the microring resonator [4]. The refractive index of silicon changes with the carrier density due to the plasma dispersion effect, resulting in the desired resonance tuning.

In the reconfigurable switch, two types of resonance tuning will be used. One is for the switching controlled by the logic signal, and the other is to change the operation mode of the switch. Figures 4(c)–4(e) show a way to realize the three operation modes of the reconfigurable switch. The logic signal tunes the resonant wavelength between λ_0 (when the logic signal is '0') and λ_1 (when the logic signal is '1'). The position of λ_0 with respect to the laser wavelength λ_L is controlled by the reconfiguration signal. When λ_L aligns with λ_1 (see Fig. 4(c)), the switch is in the block/pass mode. When λ_L aligns with λ_0 (see Fig. 4(d)), the

switch is in the pass/block mode. When λ_L aligns with neither λ_0 nor λ_1 (see Fig. 4(e)), the switch is in the pass/pass mode.
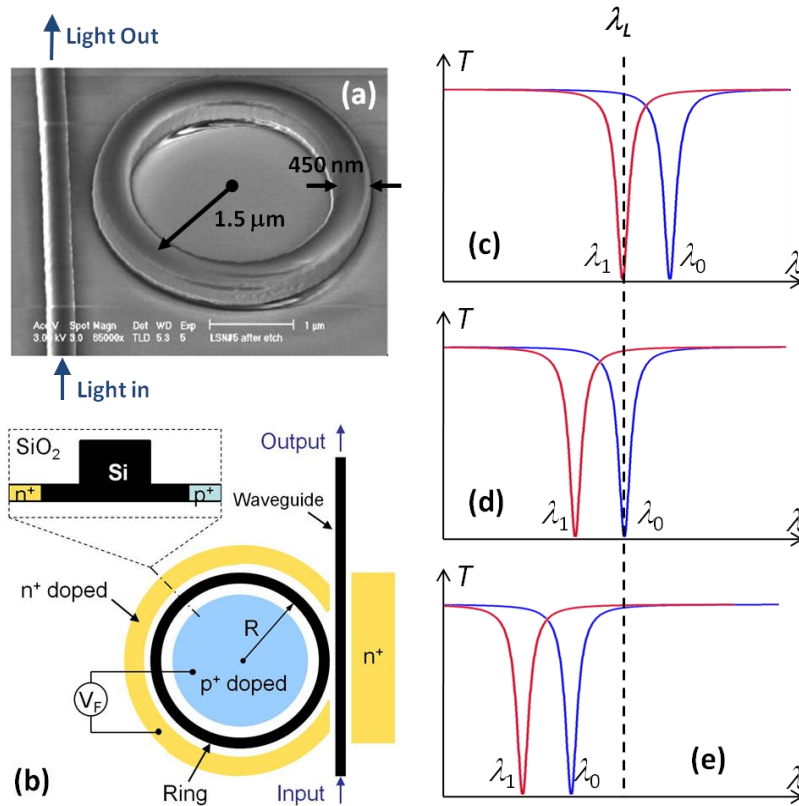

Fig. 4. The structure and operation modes of a reconfigurable 1×1 switch based on a silicon microring resonator. (a) An SEM picture of a silicon microring resonator side coupled to a silicon strip waveguide. (b) A diagram of a silicon microring modulator with a p-i-n junction built across the ring [4]. This is one of the mechanisms that can be used to tune the resonance of the ring with high speed. (c) The transmission spectra of a switch in block/pass mode for light with the wavelength of λ_L. Red line is the spectrum when the logic signal is '1', and λ_1 marks the resonant wavelength at this state. Blue line is the spectrum when the logic signal is '0', and λ_0 marks the resonant wavelength at this state. (d) The transmission spectra of a switch in pass/block mode. (e) The transmission spectra of a switch in pass/pass mode.

The two types of resonance tuning involved in the reconfigurable switch operation have different requirements. The switching operation needs to be very fast so that a logic signal with a high bit rate can be processed. The tuning mechanisms based on free carriers are most suitable in this situation, since switching (amplitude modulation) speeds of 40 Gbit/s have been demonstrated [22]. The tuning for reconfiguration does not require a high speed, but a wider tuning range is needed. While the free-carrier-based tuning can still be used for reconfiguration, slower and lossless tuning mechanisms such as those based on the thermo-optic effect and those based on micro-mechanical structures can also be employed. The advantage of thermo-optic tuning lies in its structural simplicity, while the main strength of the micro-mechanical tuning is that it has no steady-state power consumption.

Silicon compatible electro-absorption (EA) structures [23] can also be used as the 1×1 switches in the proposed architecture. To do that, however, the insertion loss of the EA switch has to be reduced to a fraction of a dB, so that cascading a large number of EA switches is possible.

5. Architecture with expanded unit cell

While any logic function can be expressed in the sum-of-products format, the number of products that needs to be calculated can be very large for some logic functions. In the worst case scenario, a logic function with N inputs requires $\sim 2^N$ products to be calculated.

For some of these functions, we can calculate them with a much more compact circuit if we can implement XOR and XNOR gates in addition to the AND gates we show above. When adding the capability of XOR and XNOR gates, we want to maintain the cellular structure of the circuit, which is necessary to achieve maximal reconfigurability. We will show in this section an expanded unit cell that can be reconfigured to perform both AND/NAND and XOR/XNOR operations.

5.1 The expanded unit cell

The expanded unit cell is composed of two parallel waveguides, a 2×2 switch and a 1×1 switch. Figure 5(a) shows the structure of an expanded unit cell implemented with microring resonators, and Fig. 5(b) is a block diagram of the unit cell. Figure 5(d) gives an example showing how the expanded unit cells are connected to form a switch fabric. As for the two waveguides in the expanded unit cell, the top waveguide is the main line that carriers the logic signal, while the bottom waveguide is an auxiliary waveguide used to realize the XOR and XNOR functions. The two coupled microring resonators in Fig. 5(a) act as a forward-dropping 2×2 switch [24] between the two waveguides, a pair that redirects light to the bottom waveguide when they are on resonance (*cross* state), and keeps light in the input waveguide when they are off resonance (*bar* state). The 1×1 switch is a microring resonator coupled only to the bottom waveguide. By passing or blocking optical waves in the bottom waveguide, it changes the logic function that the unit cell performs.

The 2×2 switches are controlled by both a logic signal and a reconfiguration signal, in the same way as that described in Section 4 for the single microring resonators. By adjusting λ_0 of these two resonators, this switch can be reconfigured into three modes: the bar/cross, cross/bar and bar/bar modes. The 1×1 switch in this unit cell, on the other hand, is not controlled by the logic signal. Its state is determined only by a reconfiguration signal.

When the 1×1 switch is in the *pass* state, this unit cell will calculate an XOR or XNOR function between its logic input and the logic input of the next unit cell. Figure 5(c) shows how an XOR between two logic inputs A and B is calculated. The 2×2 switches in the two unit cells are in the cross/bar mode and the bar/cross mode respectively. Therefore, only when the two logic signal *A* and *B* are different, the two 2×2 switches will be both in the *bar* state or both in the *cross* state. When both switches are in the *bar* state, light goes directly through the top waveguide, and when both switches are in the *cross* state, light passes the first 1×1 switch and goes back to the top waveguide of the second unit cell. In either case, a high optical transmission at the top waveguide is obtained. When *A* and *B* are the same, on the other hand, light goes to the bottom waveguide after the second 2×2 switch, and is then blocked by the second 1×1 switch.

When the 1×1 switch in an unit cell is in the *block* state, the unit cell acts as an 1×1 switch for the top waveguide: it blocks light when the 2×2 switch is in the *cross* state, and it passes light when the 2×2 switch is in the *bar* state. In this way, the unit cell performs AND functionality just like the 1×1 switches described in the previous section.
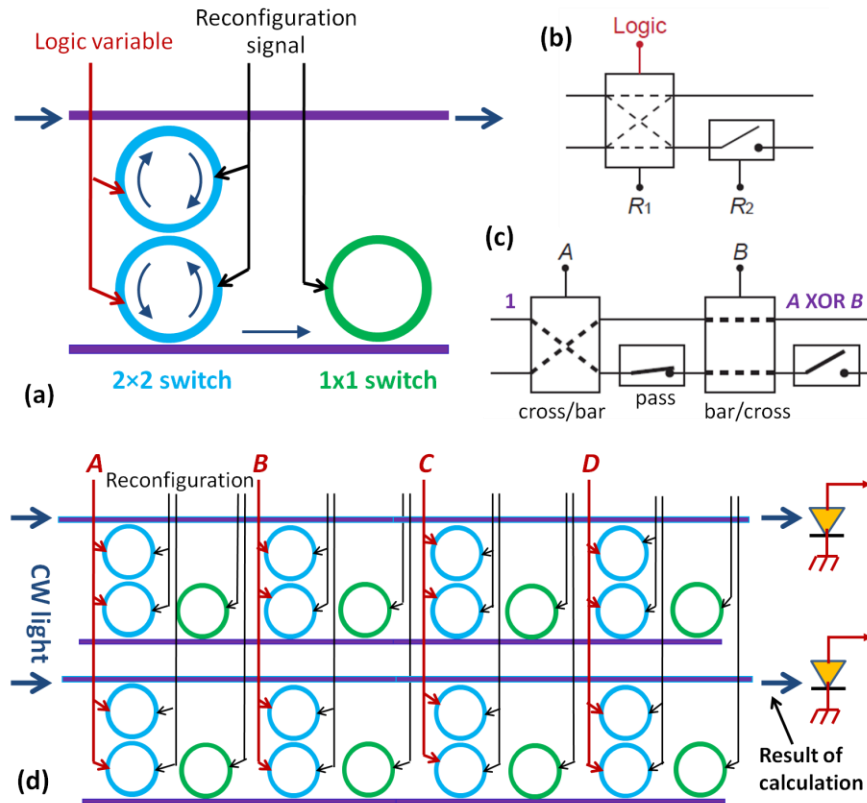
Fig. 5. The structure of the expanded unit cell. (a) The structure of an expanded unit cell based on tunable microring resonators. The two coupled microring resonators between two parallel waveguides forms a 2×2 switch. The dark blue arrows indicate the travel direction of light. (b) A block diagram of the expanded unit cell, which is composed of a 2×2 switch controlled by a logic signal and a reconfiguration signal R_1, and a 1×1 switch controlled by another reconfiguration signal R_2. (c) A block diagram of an XOR gate formed by two unit cells. The diagram shows the operation mode of each switch in order to perform the XOR operation. (d) A 2×4 switch fabric composed of two arrays with four unit cells in each array. Each array can calculate a generalized product of four logic inputs (A, B, C and D).

The logic function that an array of cascaded unit cells (as shown in Fig. 5(d)) can calculate is in the form of XOR/XNOR operations between neighboring logic inputs that are linked by AND operations (e.g. (A XOR B) AND (C XNOR D)). We will call this type of function a generalized product in the following subsections. Any logic function can be expressed as a sum of generalized products of the logic inputs. This is true because the product we considered in the previous section is just a subset of the generalized product we defined here. In the next two subsections, we will show two examples in which the capability of performing XOR and XNOR functions helps to significantly reduce the size of the directed logic.

5.2 Four-bit comparator

Since comparing two bits is inherently an XOR/XNOR operation, the availability of XOR and XNOR gates makes it much easier to implement a comparator than if only AND gates are available. Figure 6(a) shows how to compare two 4-bit numbers X and Y. Three logic outputs indicating whether or not $X = Y$, $X > Y$ and $X < Y$ are provided. In the figure, the symbols that represent the six different operation modes of each unit cell are explained in the table to the right of the figure. To compare two N-bit numbers (a total of $2N$ logic inputs), only $2N$-1

generalized products are needed. If we use the sum-of-product method as shown in the previous section, up to $3 \times 2^N - 2$ products are needed.

(a)

$y_3\ x_3\ y_2\ x_2\ y_1\ x_1\ y_0\ x_0$

$X=Y\ X>Y\ X<Y$

Light In

OE Conversion

$X = x_3x_2x_1x_0\ ;\ \ Y = y_3y_2y_1y_0$

Light In

Shape	2×2	1×1
▶	bar/cross	pass
▷	cross/bar	pass
■	bar/cross	block
◻	cross/bar	block
⋯	bar/bar	block
○	bar/bar	pass

(b)

$y_3\ x_3\ y_2\ x_2\ y_1\ x_1\ y_0\ x_0$

$z_4\ z_3\ z_2\ z_1\ z_0$

Light In

OE Conversion

Bi-unit modes	logic
▶◻ or ▷■	A XOR B
▶■ or ▷◻	A XNOR B
■ ■	A AND B
◻ ■	$\overline{A}$ AND B
■ ◻	A AND $\overline{B}$
◻ ◻	$\overline{A}$ AND $\overline{B}$

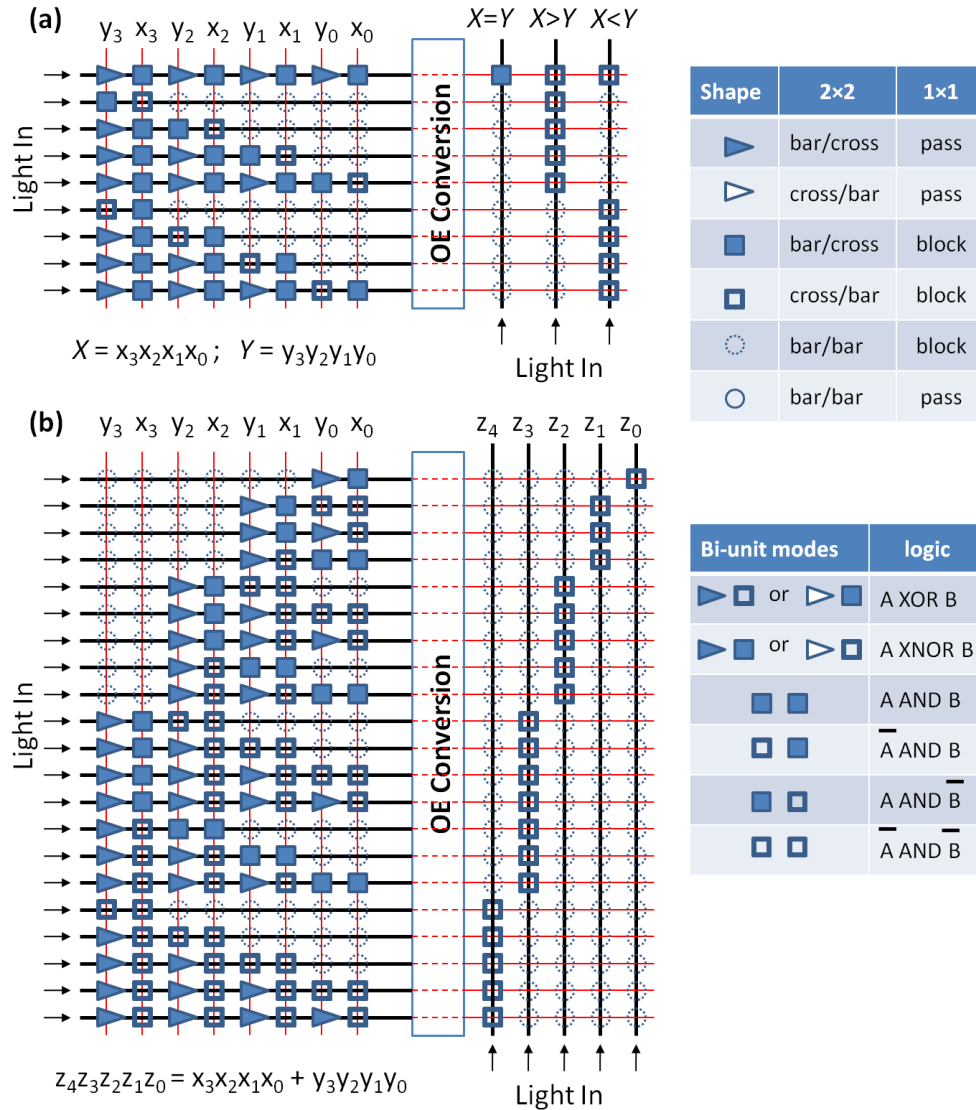$z_4z_3z_2z_1z_0 = x_3x_2x_1x_0 + y_3y_2y_1y_0$

Light In

Fig. 6. Circuit diagrams of: (a) a comparator for two 4-bit binary numbers, and (b) a full adder of two 4-bit binary numbers.

5.3 Four-bit full adder

An adder is another example where the availability of XOR gates (an XOR gate is also a 1-bit half-adder) in the expanded unit cells can significantly reduce the complexity of the directed logic circuits. The circuit is shown in Fig. 6(b). The output of the circuit is a 5-bit binary number that is the sum of two 4-bit binary numbers. To add two N-bit binary numbers, $N^2 + N + 1$ generalized products are needed. In comparison, the products that need to be calculated when the adder is expressed in the sum-of-product form is on the order of 2^{2N-1}, which is significantly larger than $N^2 + N + 1$ even when N is not very large.

5.4 Discussion

As shown in the two examples above, for some logic functions, using the expanded unit cell can significantly reduce the number of (generalized) products that need to be calculated. Even though each expanded unit cell needs 3 times more micro-resonators than the 1×1 switch unit cell used in Section 4, using the expanded unit cell can still result in a significant reduction in the total number of micro-resonators—which implies a corresponding reduction in both size and power consumption of the circuit.

However, using the expanded unit cell brings back a disadvantage in terms of latency. As explained in Section 2, when light travels to the cross port of a 2×2 switch based on micro-resonators, it experiences an additional delay determined by the photon lifetime of the micro-resonator. By using only 1×1 switches, this delay is avoided. Since the expanded unit cell uses a 2×2 switch, it brings back the additional delay when XOR and XNOR operations are performed, which erodes into the latency advantage of directed logic paradigm. There is thus a trade-off between the size of the circuit and the latency. To limit the maximal latency, one may need to put an upper limit on the number of XOR/XNOR gates that can be cascaded along a waveguide, even though that may require a larger number of generalized products to be calculated.

6. Alternative implementations

The two-stage electro-optic logic architecture shown above is not the only way to implement a reconfigurable cellular DL. Here we show some alternative approaches, and we will discuss their pros and cons compared to the two-stage architecture we show above.

6.1 All-optical logic circuit

The logic architecture presented here can also be used to build an all-optical logic. This is done by replacing the electro-optic switches with all-optic switches. It has been shown that, in micro-resonators, one optical beam can control the transmission of another optical beam (a nonlinear interaction). For example, the intense control light generates free carriers in the microresonator due to two-photon absorption in silicon and shifts its resonance through the plasma dispersion effect. All-optical switches with fast speed and low switching power have been demonstrated [25].

In an all-optical logic circuit, the O/E conversion module is no longer needed. The optical output of the first stage can, in principle, be directly used to control the switches in the second stage. To do that, however, one needs to make sure the optical output of the 1st stage has enough energy to drive the switches in the 2nd stage. This can be done by using an all-optical switch with lower switching power (higher Q and/or smaller mode volume) for the 2nd stage.

6.2 Circuit based on incoherent sum

In this subsection, we show an alternative way to calculate the sums (the OR function). In the architectures presented in previous sections, the sums are calculated by a 2nd-stage switch fabric that performs an inverted product. The alternative way is to calculate the sum by directly collecting the optical output of all the waveguides in the 1st-stage switch fabric and assigning the output as logic '1' if the total power is above the level of a single active waveguide.

If the light from all the waveguides are joined together coherently, e.g. with directional couplers, the combined power will depend on the phase relationship between light from different waveguides, which is hard to control precisely. A more practical approach is to add the optical power together incoherently. Here we show two ways to perform the incoherent sum.

6.2.1 Parallel connected photodetectors

One way to perform an incoherent sum is to convert the optical output of each waveguide to photocurrent and then to add up all of the individual photocurrents with a parallel-connected photodetector array as shown in Fig. 7. If the combined photocurrent is higher than that expected when only one of the optical waveguide has high output, it will trigger the receiver circuit to define the output logic as '1'. This performs an OR (sum) function. Since light waves in different waveguides do not interact with each other directly, no interference between them would occur.

By eliminating the second stage of switch fabric in the previous design, this logic structure reduces the complicity, size and power consumption of the logic circuit by about half. It can reduce the latency even more significantly, since in the two-stage design, the path of light is generally longer in the 2nd stage (determined by the number of products) than that in the 1st stage (determined by the number of inputs). On the other hand, this incoherent sum approach put more stringent requirements upon the extinction ratio of the optical switches, the uniformity of the optical power in each waveguide and the dark current of the photodetectors. When the leaked light from the turned-off switches and the dark currents of all the parallel connected photodetectors are added up, they have to be lower than the lowest signal level when only one waveguide is active.
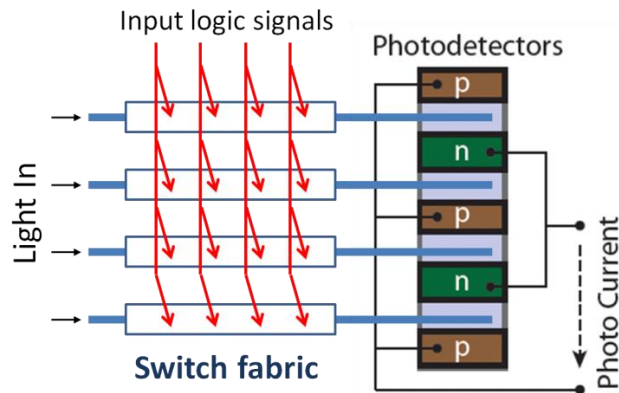

Fig. 7. The diagram of a four-input directed-logic circuit where parallel connected p-i-n photodetectors sum optical output signals from the switch fabric that calculates products or generalized products of the logic input. The switch fabric has the same structure as the 1st-stage switch fabric shown in either Section 3 or Section 5.

6.2.2 Multi-spectral logic: wavelength-multiplexed circuits

Another way to perform the incoherent sum is to inject multiple wavelengths into the fabric with a comb laser or a set of lasers at different wavelengths. Then we can obtain a 1st-stage fabric that has (for example) a different wavelength in each waveguide. Figure 8(a) shows the structure of such a circuit. The 1st-stage switch fabric used to calculate the products (or the generalized products) has the same structure as before, but the switches on different waveguides operate at different wavelengths. The calculated products are then carried by light at different wavelengths and are selectively coupled to an output waveguide by a tunable microring resonator. This multi-spectral approach eliminates the middle O/E conversion module.

To give a more specific example, Fig. 8(b) shows a 4-bit comparator circuit that has the same functionality as that shown in Fig. 6(a). The optical source of this circuit is a multi-wavelength laser such as those demonstrated in [26–29]. Different wavelengths are dropped into different waveguides by microring resonators having different diameters. After light

passes through a (horizontal) switch array, it will be redirected to an output (vertical) waveguide if the ring resonator at the waveguide's cross point is on resonance with the light (orange circles). If the microring resonator at the cross point is tuned away from the wavelength of light in the horizontal waveguide (dashed green circles), light will not be collected by that output waveguide.

The broadband photodetector at the end of an output waveguide will absorb photons at all source wavelengths and create a photocurrent that sums the optical outputs from the horizontal waveguides that couple to that vertical output waveguide. If the photocurrent is higher than that expected when one of the horizontal waveguide has high output, it will trigger the receiver circuit to define the output logic as '1'. This performs the OR (sum) function of the products calculated by the coupled horizontal waveguides.
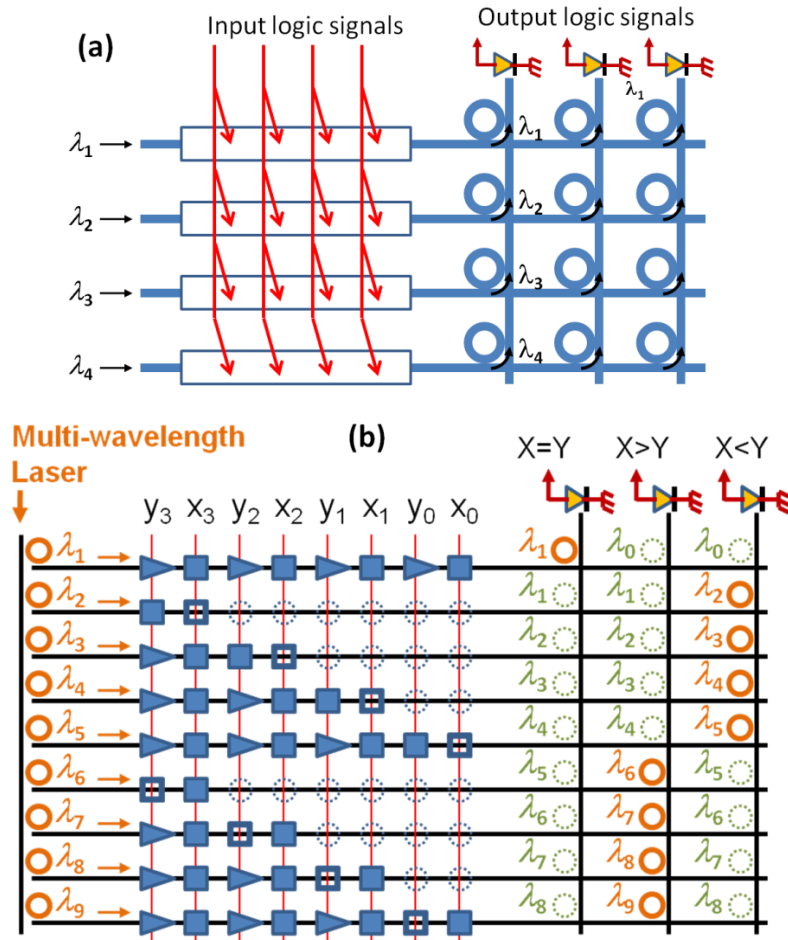

Fig. 8. (a) The diagram of a four-input multi-wavelength DL circuit that performs sum operation by collecting optical output at different wavelengths into one waveguide with the tunable microring resonators. (b) A diagram of the multi-wavelength directed logic circuit that performs the comparison of two 4-bit binary numbers.

6.2.3 Discussion

Compared to the two-stage switch fabric designs shown in Sections 3 and 4, the incoherent sum methods remove the middle O/E conversion block and reduce the number of optical switches used in the directed logic circuit. Therefore, they can have advantages in power consumption, size and latency. However, both incoherent sum methods shown above require

high extinction ratio for the switches and a uniform distribution of light to every waveguide that calculates products. Since experimentally demonstrated optical switches based on microring resonator generally have extinction ratios below 20 dB, the number of products that can be summed up this way is well below 100.

In order to achieve better scalability, the incoherent sum methods can be combined with the 2nd-stage switch fabric shown in the previous sections. If a large number ($m \times n$) of products need to be summed, they can be grouped into n groups, where m products in each group are summed incoherently to create a single control signal, and the n control signals from the n groups are then summed with a switch fabric that has the same structure as the 2nd-stage switch fabric shown in Sections 3 and 4.

7. Conclusion

We propose here a cellular optical DL logic architecture that is reconfigurable and scalable. This architecture is built upon ultra-compact silicon photonic devices that offer the capability of large-scale integration. Based on this architecture, we show the circuits that realize several common logic functions, including an encoder, a multiplexer, a full adder and a comparator. We also show several alternative implementations of the proposed architecture, whose pros and cons are discussed.

Acknowledgement